REMARKS

Claims 1-8 and 10-27 will be pending upon entry of the present amendment. Claims 1, 5, 8, 10-16, and 21-24 are being amended. Claims 25-27 are new.

Allowable Subject Matter

The applicants appreciate the indication that claims 6, 14-15 and 23 are directed to allowable subject matter. New independent claim 25 is directed to claim 6 prior to the amendment of claim 1, from which claim 6 depends. New independent claim 26 is directed to claim 14 prior to the amendment of claim 10, from which claim 14 depends. New claim 27 is dependent on claim 26. Claim 23 is being placed in independent form. Thus, claims 25-27 are in condition for allowance.

Objections

Claim 24 is objected to because of an informality. The informality is corrected by the amendments above.

Rejections Under 35 U.S.C. §112

Claims 1-7 are rejected as being indefinite due to a typographical error in claim 1. The typographical error is corrected by the amendments above.

Rejections Under 35 U.S.C. §102

Claims 10-13, and 16-20 were rejected under 35 U.S.C. §102(e) as being anticipated by Robinson (U.S. Patent No. 5,682,497).

Robinson is generally directed towards a method for managing a file system in the Flash memory on a personal computer, such as a personal computer running MS-DOS. Robinson discloses that compression and collapsing of the linked list chains inherent in a file system decreases the amount of time required to subsequently retrieve the file, and increases utilization of the Flash memory array (*see e.g.*, Robinson, col. 2, lines 45-49; col. 2, lines 59-65).

Robinson does not disclose the features of claim 10 as amended. Claim 10 has been amended to recite, "an internal address bus running inside the memory macrocell; an address counter receiving having an output connected to the internal address bus; and a state machine for controlling the address counter, said address counter receiving control signals from the state machine in order to control the loading of hard-coded addresses such that the corresponding pages always share the same non-changeable address." Robinson does not disclose such hard-coding of addresses. Rather, as a dynamic file system, such allocations are dynamic (*see, e.g.*, Robinson, col. 6, lines 25-32; col. 9, lines 18-21). Further, Robinson makes no mention of such a state machine for controlling an address counter. Accordingly, Robinson does not anticipate claim 10, and claim 10 is thus allowable.

Robinson does not disclose the features of claim 16 as amended. Claim 16 has been amended to recite, "sectors wherein such assignment is hard-coded such that the corresponding pages always share the same non-changeable address ... and updating a state machine ... updating the state machine ... determining from the state machine ... ." As discussed with regards to claim 10, Robinson does not disclose such hard-coding of addresses, nor does it disclose such a state machine. Accordingly, Robinson does not anticipate claim 16, and claim 16 is thus allowable.

Rejections Under 35 U.S.C. §103

Claims 1-5, 7-8, 21-22, and 24 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lee (U.S. Patent No. 5,956,268) in view of James (U.S. Patent No. 5,966,723).

Lee '268 and James fail to teach or suggest the invention recited in claim 1. Claim 1 recites, "an integrated circuit having a microcontroller, the memory macrocell ... structured to emulate EEPROM byte alterability corresponding to an EEPROM memory array having a selected number of EEPROM memory cells, the selected number of EEPROM memory cells being emulated being fewer than the selected number of NOR Flash memory cells."

Lee '268 fails to teach or suggest a device structured to emulate EEPROM byte alterability. While Lee '268 mentions that a sector may contain any number of transistors, the sizing of a sector to contain only a single byte of data, as required to allow byte alterable, would

remove many of the size and simplicity advantages inherent in Flash memory of larger sector size. Such a single byte sector memory device would not have emulated EEPROM byte alterability, but would have true EEPROM byte alterability, and would be an EEPROM rather than a Flash memory device.

In addition, Lee '268 fails to teach or suggest a device in which the selected number of EEPROM memory cells being emulated is few than the selected number of NOR Flash memory cells. The hypothetical Lee '268 memory device with a single byte sector would not result in the number of emulated EEPROM memory cells being emulated being fewer than the number of NOR Flash memory cells. Rather, there would be a one to one relationship between the number of memory cells emulated and the number being used. Accordingly, it would not result in a device wherein the selected number of EEPROM memory cells being emulated being fewer than the number of NOR Flash memory cells as recited by claim 1.

In addition, the Examiner admits that Lee '268 does not teach or suggest an integrated circuit having a microcontroller, but mistakenly asserts that James does teach such a microcontroller. It is commonly known to persons skilled in the art, that a microcontroller is defined as a microprocessor on a single integrated circuit intended to act in an embedded system (*see e.g.*, dictionary.com, attached). A microprocessor is defined as an integrated circuit having an entire CPU on a single chip (*see e.g.*, dictionary.com, attached). James teaches none of the above-mentioned features of a microcontroller.

The Examiner refers to col. 3, line 64 through col. 4, line 22 James as teaching the use of a microcontroller, but that section of James fails to teach or suggest a microcontroller. For example, that section of James mentions a "serial interface activation circuit" and a "device state machine," those devices are not microcontrollers. That is, neither device is "an entire CPU on a single chip," as discussed above for a microcontroller.

For the reasons discussed above, Lee '268 and James do not teach or suggest the features as recited by claim 1. Thus, claim 1 is allowable. Claims 1-5, 7 and 21 depend on claim 1, and thus, are likewise allowable.

Lee '268 and James also fail to teach or suggest the invention recited in claim 8. Claim 8 recites, "an integrated circuit that also includes a microcontroller and a NOR Flash

memory structure formed by a predetermined number of sectors, ... and updating the emulated EEPROM memory portion programming different memory locations in a single bit mode, wherein at a page update selected page data are moved to a next free block and, when an emulated EEPROM sector is full, all the pages are swapped to another emulated EEPROM sector." As discussed above, Lee '268 and/or James fail to teach or suggest an integrated circuit having a microcontroller or a device that is structured to emulate EEPROM byte alterability.

In addition, Lee '268 and James fail to teach or suggest the recited page updating and swapping. The Examiner admits that Lee '268 does not teach or suggest the page updating and page swapping to another emulated EEPROM sector, but mistakenly asserts that James does. James teaches a method to shift data into or out of the Flash memory device (*see, e.g.*, James, col. 5, line 10 – col. 6, line 12). No mechanism is provided to shift page data to a next block within the memory array. Moreover, such shifting into or out of a memory device does not involve swapping all of the pages of a first sector to a second sector when the first sector is full.

Accordingly, Lee '268 and/or James do not teach or suggest the features as recited by claim 8. Thus claim 8 is allowable.

Lee '268 and James also do not teach or suggest the invention recited in claim 22, as amended. Claim 22 recites and emulated EEPROM memory array that includes a microcontroller and "an address counter whose output is coupled to an internal address bus of the memory array for tracking and controlling the address at which emulated EEPROM data is stored ...." The cited prior art does not suggest these features.

The Examiner states that col. 3, lines 22-30 of James teaches a microcontroller. This is not understood. The cited paragraph introduces a non-volatile memory device having a serial interface and lists exemplary devices to which such a serial interface may be adapted. The cited paragraph makes mo mention of a microcontroller.

Further, Lee '268 and/or James fail to teach an address counter for tracking and controlling the address at which emulated EEPROM data is stored. James teaches an "Address Register", (*see, e.g.*, James, Figure 2, element 6; Figure 2, "TO ADDRESS REGISTER"; col. 4, line 6), as well as a "command/address shift register, (*see, e.g.*, James, Figure 2, element 17; col. 5, line 19). These registers are not address counters. It is commonly known in the art that an

address counter must include both a storage element as well as means to increment or decrement the storage element. No such means are taught or suggested for incrementing or decrementing the address register or the command/address shift register. Accordingly, these shift registers cannot be the address counters cited by the Examiner.

James does not teach an address counter whose output is coupled to an internal address bus of the memory array for tracking and controlling the address at which emulated EEPROM data is stored, as recited by claim 22. While James teaches an address counter for automatically incrementing the address at which data is read or programmed during sequential serial read or write operations (*see, e.g.*, James, col. 9, lines 15-18), such address counter is not the address counter recited by the present application, as it is not coupled to the internal address bus for tracking and controlling the address at which emulated EEPROM data is stored.

Accordingly, Lee '268 and James do not teach or suggest the features as recited by claim 22. Thus claim 22 is allowable.

Claim 24 recites, "at least two of the sectors being structured to emulate an EEPROM having byte erasability, the emulated EEPROM bytes comprising substantially fewer memory cells than an entire sector." As discussed in regards to claim 1, Lee '268 and/or James fail to teach or suggest a device that is structured to emulate an EEPROM having byte erasablity. Both Lee '268 and/or James teach sector erasability, and do not teach or suggest such emulated EEPROM erasability. As further discussed in regards to claim 1, Lee '268 and/or James fail to teach or suggest a device wherein the number of emulated EEPROM bytes comprised substantially fewer memory cells than an entire sector, as recited by claim 24. Accordingly, Lee '268 and/or James do not teach or suggest the features as recited by claim 24. Thus claim 24 is allowable.

Conclusion

Overall, none of the references singly or in any motivated combination disclose, teach, or suggest what is recited in the independent claims. Thus, given the above amendments and accompanying remarks, the independent claims are now in condition for allowance. The

dependent claims that depend directly or indirectly on these independent claims are likewise allowable.

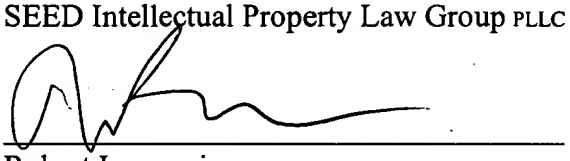
If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (206) 622-4900.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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